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Mark L. Watson
BLAKELY, SOKOLOFF, TAYLOR & ZAFMANN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
TSAI, HENRY	
ART UNIT	**PAPER NUMBER**
2183	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/842,536	Applicant(s) VAVRO, DAVID K.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,11-13 and 19-28* is/are rejected.

7)☒ Claim(s) *4-10 and 14-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/25/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 1, line 4, "an execution unit coupled to the instruction buffer and the first MO buffer" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Note in Fig. 3, MO BUFFER 320(1) and MO BUFFER 320(2) are not coupled to INSTRUCTION EXECUTION 340.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to because in Fig. 3, "INSTRUCTION DECODE" should read -- INSTRUCTION DECODE MODULE--; and "INSTRUCTION EXECUTION" should read -- INSTRUCTION EXECUTION UNIT -- in order to be consistent with the description of the specification. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid

abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 16-18, 23 and 28 are objected to because of the following informalities:

in claim 16, line 1, "5" should read --15-- since a DSP is not the claim 5 invention; and

in claim 23, line 3, before "if", should --and-- be inserted ?

in claim 28, line 4, before "if", should --and-- be inserted ?

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. Claims 19-23 and 26-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 19, line 5, it is not clear what is meant by "retrieving the buffer from a second buffer" since "retrieving the buffer" was not previously defined.

In claim 21, line 6, it is not clear why the first instruction is retrieved from the second buffer since in the preceding step as shown line 5, the first instruction is stored in the first buffer instead of the second buffer. Similar problems exist in the other claim 26.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 19-21 and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Shiell et al. (U.S. Patent No. 5,935,241) hereafter referred to as Shiell et al.'241

Referring to claim 1, Shiell et al.'241 discloses as claimed a processing element comprising: an instruction buffer (see Fig. 2, inside instruction buffer and control 60 which is in a fetch unit 26, see also Col. 9, lines 30-31); a first most often (MO) buffer (level 1 instruction cache 16i see Fig. 1) coupled to the instruction buffer (see Fig. 2); and an execution unit (comprising ALU 0 42_0, ALU 1 42_1, see Fig. 1) coupled to the instruction buffer (see Fig. 2, inside instruction buffer and control 60) and the first MO buffer (level 1 instruction cache 16i see Fig. 1), wherein the execution unit is adaptable to execute instructions stored within the first MO buffer (level 1 instruction cache 16i see Fig. 1) based upon a first predetermined profile (cache "miss" in level 1 instruction cache is best reasonably and broadly interpreted as the first predetermined profile).

As to claim 2, Shiell et al.'241 also disclose: a second MO buffer (level 2 instruction cache 11 see Fig. 1) coupled to the instruction buffer (see Fig. 2, inside instruction buffer and control 60) and the execution unit (comprising ALU 0 42_0, ALU 1 42_1, see Fig. 1), wherein the execution unit is adaptable to

execute instructions stored within the second MO buffer (level 2 instruction cache 11 see Fig. 1) based upon a second predetermined profile ("miss" in level 2 instruction cache).

As to claim 3, Shiell et al.'241 also disclose: a decode module (DECODE 34, see Fig. 1) coupled to the second most often (MO) buffer (level 2 instruction cache 11 see Fig. 1) coupled to the instruction buffer, the first MO buffer (level 1 instruction cache 16i see Fig. 1), the second MO buffer (level 2 instruction cache 11 see Fig. 1) and the execution unit (comprising ALU 0 42_0, ALU 1 42_1, see Fig. 1).

Referring to claims 19 and 24, Shiell et al.'241 discloses as a method comprising: receiving a first instruction at an instruction buffer (see Fig. 2, main memory 305 or inside instruction buffer and control 60 which is in a fetch unit 26, see also Col. 9, lines 30-31); determining whether the first instruction has been designated to be retrieved from a first buffer (level 1 instruction cache 16i see Fig. 1) in order to be executed; and if so, retrieving the first instruction from the first buffer (level 1 instruction cache 16i see Fig. 1); otherwise, retrieving first instruction from a second buffer (level 2 instruction cache 11 see Fig. 1). Note when the first instruction has not been in the level 1 instruction cache (such as in a cache miss situation) then the Shiell et al. system will

try to retrieve first instruction from a second buffer (level 2 instruction cache 11 see Fig. 1).

As to claims 20 and 25, Shiell et al.'241 also discloses: executing the first instruction after it has been retrieved from the first buffer (level 1 instruction cache 16i see Fig. 1).

As to claims 21 and 26, Shiell et al.'241, as best understood, also discloses: determining whether the first instruction has been designated to be stored in the first buffer if the first instruction has not been designated to be retrieved from the first buffer in order to be executed (note this is the situation when level 1 does not contain the first instruction); if so, storing the first instruction in the first buffer (level 1 instruction cache 16i see Fig. 1); and executing the first instruction after it has been retrieved from the second buffer (level 2 instruction cache 11 see Fig. 1).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be

> patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al. in view of Pechanek et al. (U.S. Patent No. 5,682,491) hereafter referred to as Pechanek et al.'491.

Shiell et al.'241 discloses the claimed invention except for being used as one of a plurality of processing elements.

Pechanek et al.'491 discloses a system (see Fig. 6-A or Fig. 7) comprising: a plurality of processing elements (such as PE-0,0; PE-0,1; PE-1,0; and PE-1,1) and each processing element has the same structure and function.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a plurality of Shiell et al.'241's systems in a processor, as taught by Pechanek et al.'491, in order to increase the processing throughput for the Shiell et al.'241's system.

Further, as shown in St. Regis Paper Co. v Bemis Co. 193 USPQ 8 (7th Cir. 1977), to duplicate parts for multiple effects generally does not provide patentable weight to the claimed invention.

As to claim 12, Shiell et al.'241 also disclose: a second MO buffer (level 2 instruction cache 11 see Fig. 1) coupled to the instruction buffer (see Fig. 2, inside instruction buffer and control 60) and the execution unit (comprising ALU 0 42_0, ALU 1 42_1, see Fig. 1), wherein the execution unit is adaptable to execute instructions stored within the second MO buffer (level 2 instruction cache 11 see Fig. 1) based upon a second predetermined profile ("miss" in level 2 instruction cache).

As to claim 13, Shiell et al.'241 also disclose: a decode module (DECODE 34, see Fig. 1) coupled to the second most often (MO) buffer (level 2 instruction cache 11 see Fig. 1) coupled to the instruction buffer, the first MO buffer (level 1 instruction cache 16i see Fig. 1), the second MO buffer (level 2 instruction cache 11 see Fig. 1) and the execution unit (comprising ALU 0 42_0, ALU 1 42_1, see Fig. 1).

Allowable Subject Matter

5. Claims 4-10, 14, and 15, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten

in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 16-18 would be allowable if rewritten to overcome the objection, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

7. Claims 22, 23, 27, and 28 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure wherein Parady'320 discloses a processor with independent OS resources also comprising instruction cache and buffer and external cache RAM which also can be considered as MO buffers as the claimed invention; Tremblay et al.'338, discloses a clustered architecture in a VLIW processor comprising instruction cache and instruction buffer in each of processing elements; and JP-6-

237377 also teaches a processor using a plurality of processing elements as shown in Fig. 1 as the claimed invention.

Contact Information

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

10. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

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applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

May 24, 2004